AMENDMENT TO THE CLAIMS

1. (Currently amended) A digital PLL device comprising:

a first selector for selecting and outputting one of a first synchronous timing signal and a second synchronous timing signal;

a comparator for detecting a phase difference between the synchronous timing signal selected by said first selector and an internal synchronous timing signal, and outputting phase correction data corresponding to the phase difference;

a hold over [[control means]] unit for outputting hold over data used for performing phase correction;

a second selector for selecting and outputting one of the phase correction data supplied from said comparator and the hold over data supplied from said hold over [[control means]] unit, said second selector selecting the output from said hold over [[control means]] unit when a hold over mode is set;

a digital VCO for creating a clock signal with a frequency corresponding to data supplied from the second selector; and

[[means]] a filter for creating an internal synchronous timing signal from the clock signal created by said digital VCO.

2. (Original) The digital PLL device according to claim 1 further comprising a controller for controlling said selectors and changing over the first synchronous timing signal to the second synchronous timing signal at switching of synchronous timing over a digital synchronous network,

said controller setting the hold over mode during the changeover of the synchronous timing over the digital synchronous network.

3. (Currently amended) The digital PLL device according to claim 2, wherein [[a]] the hold over unit [[comprising]] comprises:

an up/down counter, the addition/subtraction of said up/down counter being controlled by the phase correction data supplied from said phase comparator;

a memory for storing, as the hold over data, a count value of said up/down counter every K (integer) frames;

a memory controller for performing read control, write control, and address control of said memory; and

a decoder for decoding the hold over data read from said memory to frequency of corrections and a correction value, and outputting the number of corrections and the correction value,

wherein said memory controller performs the read control of said memory in the hold over mode, and performs the write control of said memory when the synchronous timing signal supplied from said first selector is synchronizing with the internal timing signal.

4. (Original) The digital PLL device according to one of claim 1 through claim 3 further comprising a phase adjuster for adjusting a phase of the second synchronous timing signal to a phase of the first synchronous timing signal,

wherein said first selector selects one of the first synchronous timing signal and an output signal from said phase adjuster.

5. (Original) The digital PLL device according to one of claim 1 through claim 3, wherein said phase comparator comprising:

a phase counter for counting a phase difference between the internal timing signal and the synchronous timing signal;

a phase detecting circuit for comparing a count value obtained by said phase counter with a phase reference value;

a frequency counter for counting frequency of the synchronous timing signal;

a frequency detecting circuit for comparing a count value obtained by said frequency counter with a frequency reference value;

a phase-correction-value detecting circuit for outputting phase correction data based on a comparison result by said phase detecting circuit and a comparison result by the frequency detecting circuit; and

a state transition detecting circuit for determining one of a synchronous state and an asynchronous state based on a phase condition of the synchronous timing signal and forward protection and backward protection conditions.

6. (Original) The digital PLL device according to claim 5,

wherein said phase-correction-value detecting circuit changes a phase correction amount responsive to the synchronous state and the asynchronous state.

7. (Currently amended) A digital PBX comprising:

a plurality of I/O cards interfacing with various extensions and outside lines;

a main card for controlling said plurality of I/O cards; and

a back board for performing data communications between said main card and each of said plurality of I/O cards and between said plurality of I/O cards, and voice data communication through time slots in a plurality of channels,

wherein said main card and one of said plurality of I/O cards for functioning as a master comprise a Master PLL device,

said Master PLL device comprising:

a first selector for selecting and outputting one of a first synchronous timing signal and a second synchronous timing signal;

a comparator for detecting a phase difference between the synchronous timing signal selected by the first selector and an internal synchronous timing signal, and outputting phase correction data corresponding to the phase difference;

a hold over [[control means]] unit for outputting hold over data used for performing phase correction;

a second selector for selecting and outputting one of the phase [[difference]] correction data supplied from said comparator and the hold over data supplied from said hold over [[control means]] unit, said second selector selecting the output from the hold over [[control means]] unit when a hold over mode is set;

a digital VCO for creating a clock signal with a frequency corresponding to data supplied from the second selector; and

[[means]] a filter for creating an internal synchronous timing signal from the clock signal created by the digital VCO.